SIMBIO-SYS ME

The ATF280 in the Simbio-Sys instrument of BepiColombo

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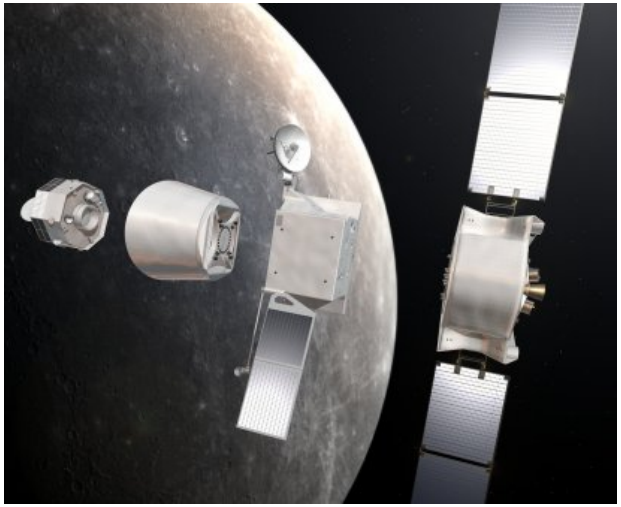
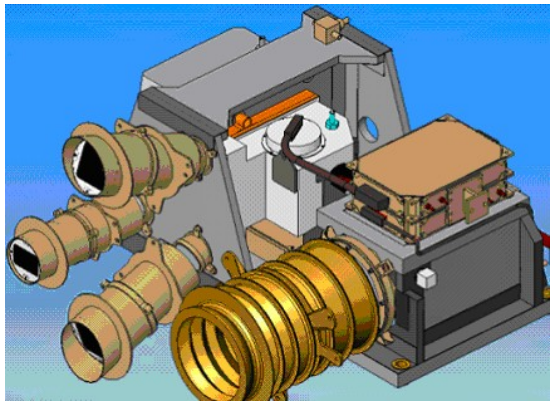
Context

SIMBIO-SYS ME

- ESA (MPO) / JAXA (MMO) cooperation for Mercury exploration
- MPO = 11 instruments
- Simbio-Sys instrument : Mercury surface study
  - HRIC : High Resolution Channel
  - STC : Stereo Channel
  - VIHI : Vis/NIR spectrometer
- IAS is Co-PI on Simbio-Sys, in charge of the DPUs of Main Electronic
- DPU (cold redundancy):
  - S/C interface
  - Cameras interface
  - **Image compression (Y.Langevin algorithm)**

  => ~70% of the data of MPO mission





Summary

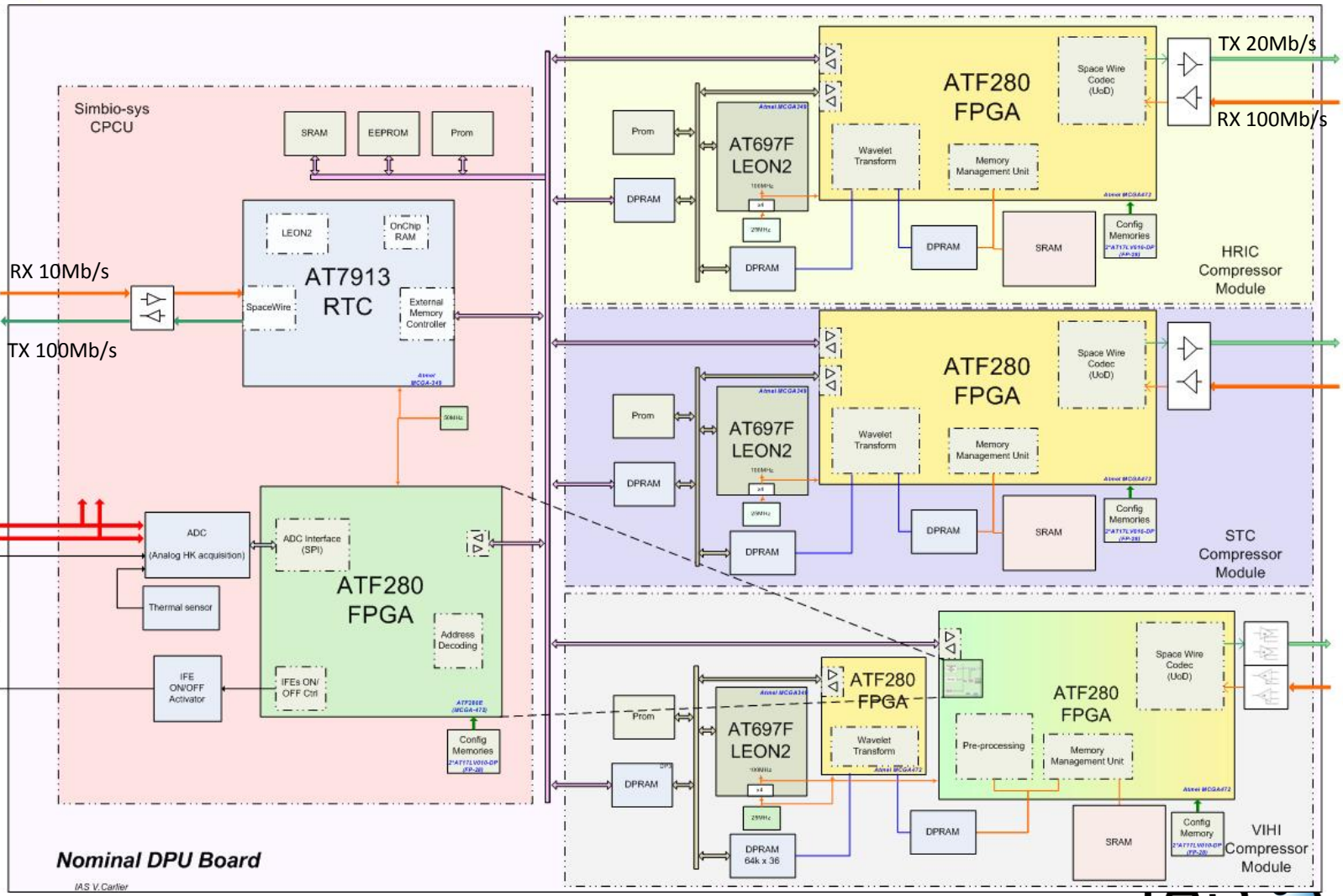
SIMBIO-SYS ME

- DPU Synoptic & components from Atmel

- FPGA implementations
  1. VIHI channel: SpaceWire & Pre-propressing
  2. VIHI channel: WT
  3. HRIC and STC channels: SpaceWire & WT

- Pictures
  - Main Electronic
  - PCB

DPU Synoptic



Atmel components

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- **Atmel RTC AT7913**
  - TM/TC interface (from SpaceCraft)
  - Data processing controller
  - SpaceWire interface with S/C : TX 100Mb/s – RX 10Mb/s
  - Clocked at 50MHz
- **Atmel FPGA ATF280**
  - SpaceWire (UoD v2.3) interface with imagers : TX 25Mb/s – RX 100Mb/s
  - Wavelet Transform : 2Mpixel/s (16Mbit/s)
  - Two 1Mbit memories (AT17LV010) cascaded per FPGA
  - Clocks :
    - System at 20MHz / 25MHz.
    - Specific small parts at 100MHz and 50MHz
- **Atmel processor AT697**
  - Tree-Coding data compression
    - from 3-bit to 1-bit per pixel
    - max throughput : 16Mbit/s
  - Clocked at 100MHz

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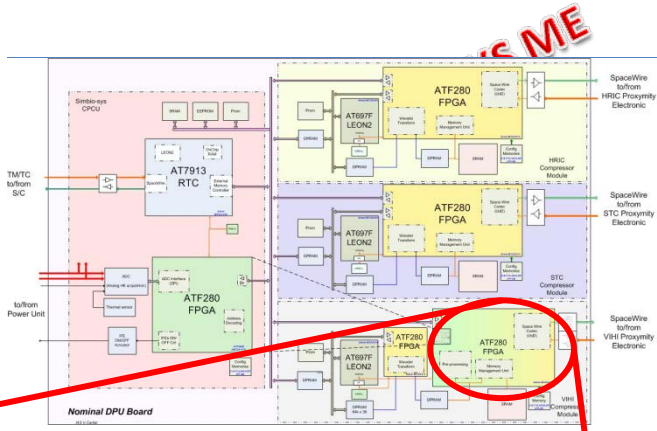
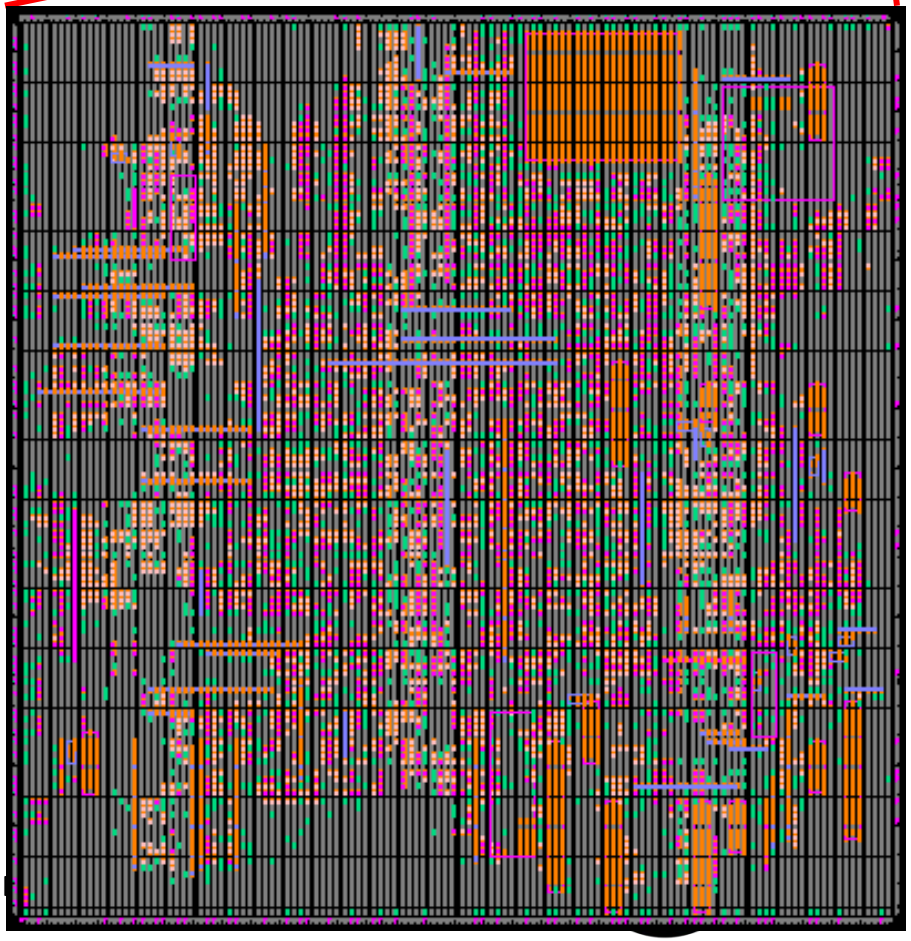
1. VIHI: SpW & Pre-proc



- Functionalities
  - SpaceWire to Proximity Electronic
  - Memory management: image acquisition/sub-pictures extraction
  - Spectral Preprocessing (before WT)
  - SPI, RTC address decoding …
- Characteristics :
  - Area = 6192 Core Cells (43.0%, with routing)
  - 196 IOs
- Design :
  - 1 multipliers : 16x21
  - Adders/Subtractors, Counters, comparators
- Clocks:
  - CPCU: 50MHz / 25MHz / 20MHz / 12MHz
  - Leon: 100MHz / 20MHz / 10MHz
  - RX_CLK: 50MHz



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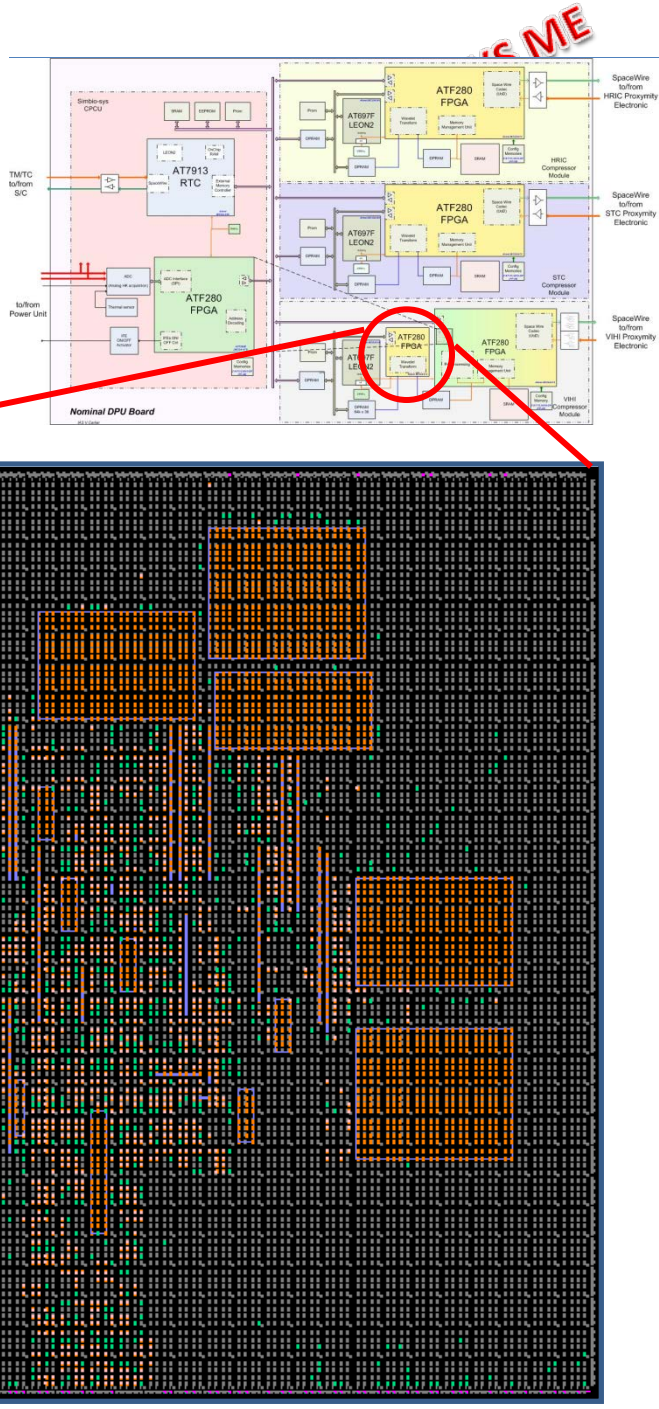
2. VIHI : WT

- Functionalities
  - Spectral Wavelet Transform
- Target : clock at 25MHz
- Characteristics :
  - Area = 4693 Core Cells (32.59 %, with routing)
  - Fmax = 26,05 MHz
  - 119 IOs
- Design :
  - 8 multipliers : 9bits x 21bits, 11x21, 12x21, 13x21, 14x21, 16x21
  - 45 Adders/Subtractors: 7 bits, 8 bits, 14 bits, (10*)21 bits, (6*)24 bits
  - Counters: 7bits, 16 bits



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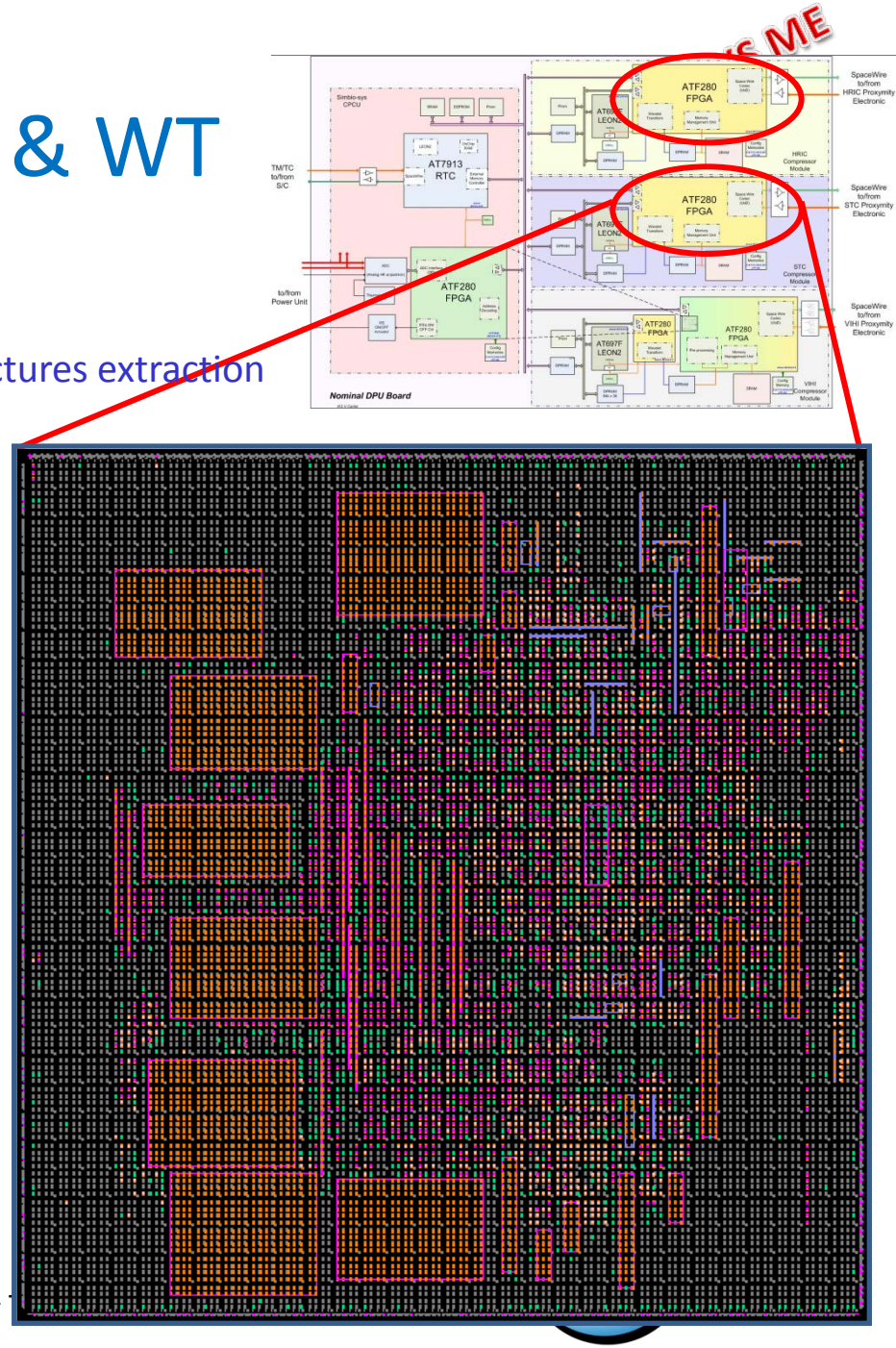
3. HRIC/STC: SpW & WT

- Functionalities:
  - SpaceWire interface with Proximity Electronic
  - Memory management: image acquisition/sub-pictures extraction
  - Spatial Wavelet Transform
- Characteristics :
  - Area = 7558 Core Cells (52.49 %, with routing)
  - 196 IOs
- SpaceWire :
  - TX : 20Mb/s (SDR, not optimized)
  - RX : 100Mb/s
  - Specific manual Place & Route
- Clocks
  - 2 primary clocks
  - 4 derived clocks

  (cf. below)



3. HRIC/STC: SpW & WT

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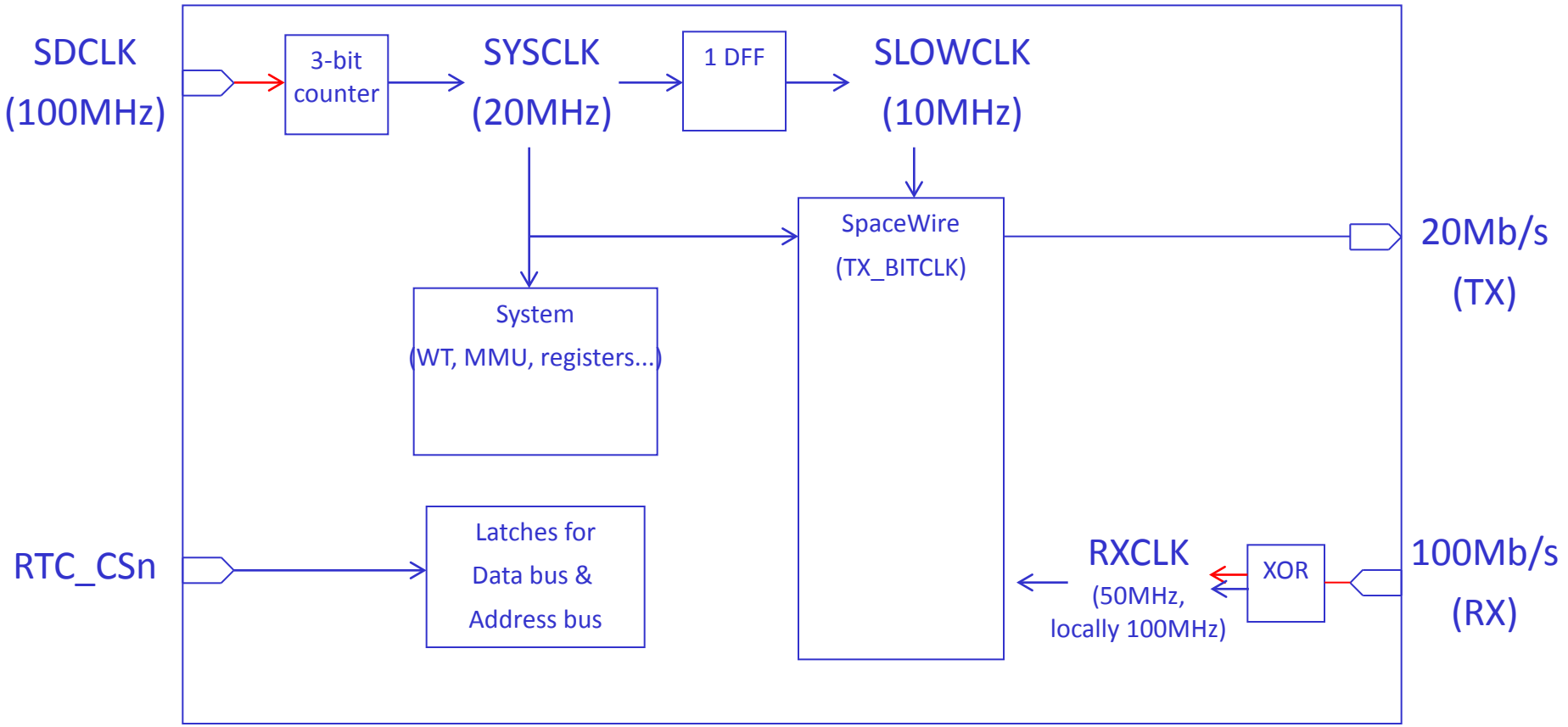
Clock distribution



3. HRIC/STC: SpW & WT

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Timings analysis (STA from IDS)

Clock name	Target	STA (IDS)	Nb of cells	
SDCLK_TC	100MHz	118.91MHz	3	All design are validated by test at target frequencies under the worst case conditions (temperature and voltage) corresponding to the mission profile.
SYSCLK	20MHz	15.62MHz	1727	
SLOWCLK	10MHz	21.66MHz	31	
TXBIT_CLK	20MHz	33.77MHz	93	
RX_CLK	50MHz	43.84MHz	106	
RTC_CSn	N/A	N/A		

3. HRIC/STC: SpW & WT

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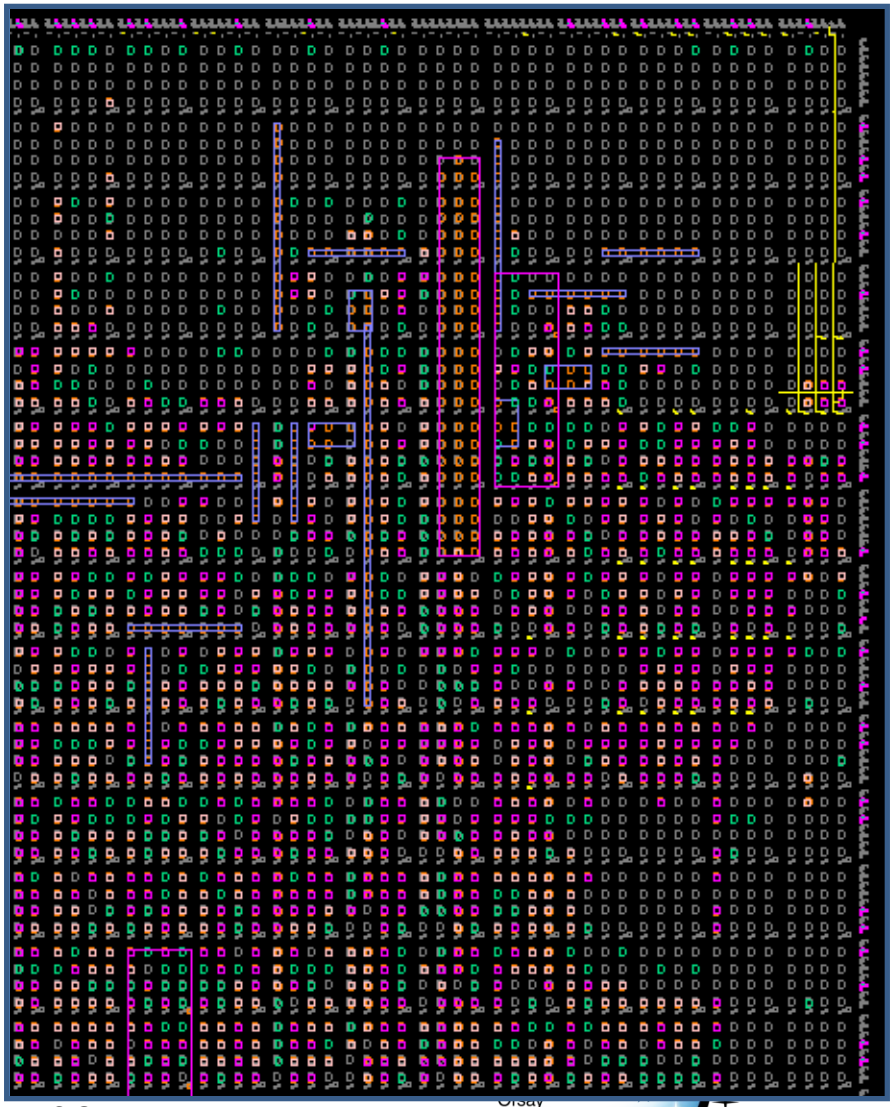
Details of the SpaceWire IP

- UoD codec v2.3 (supplied by ESA)
- Performances :
  - TX 20Mb/s (SDR)
  - RX 100Mb/s
- Specific manual Place & Route for RX data path :
  - manual placement of some cells (<10)
  - manual routing of RX_CLK :
    - * short local routing for <10 cells
    - * global routing for the rest of SpaceWire RX datapath



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Main Electronic

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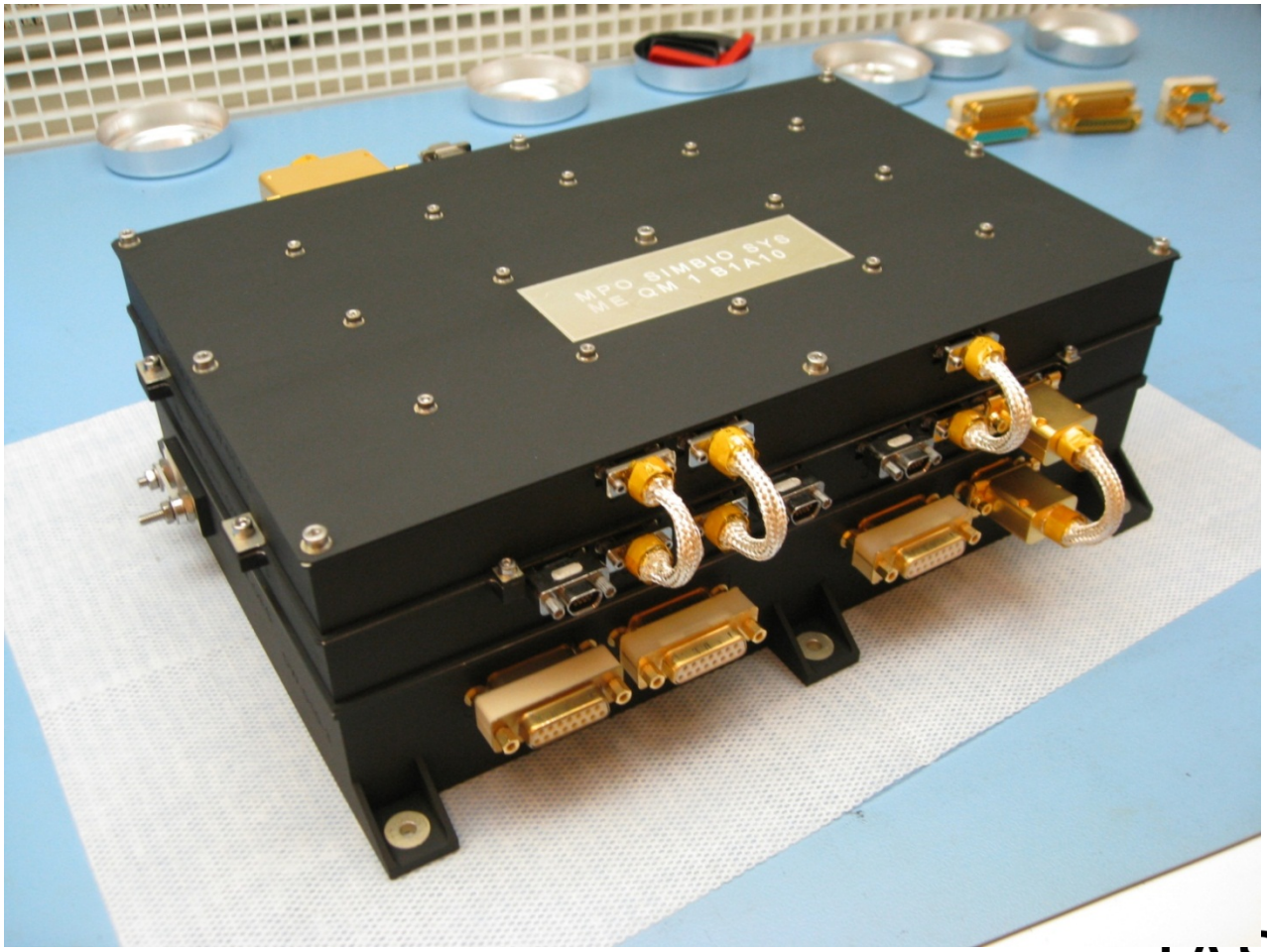

Main Electronic

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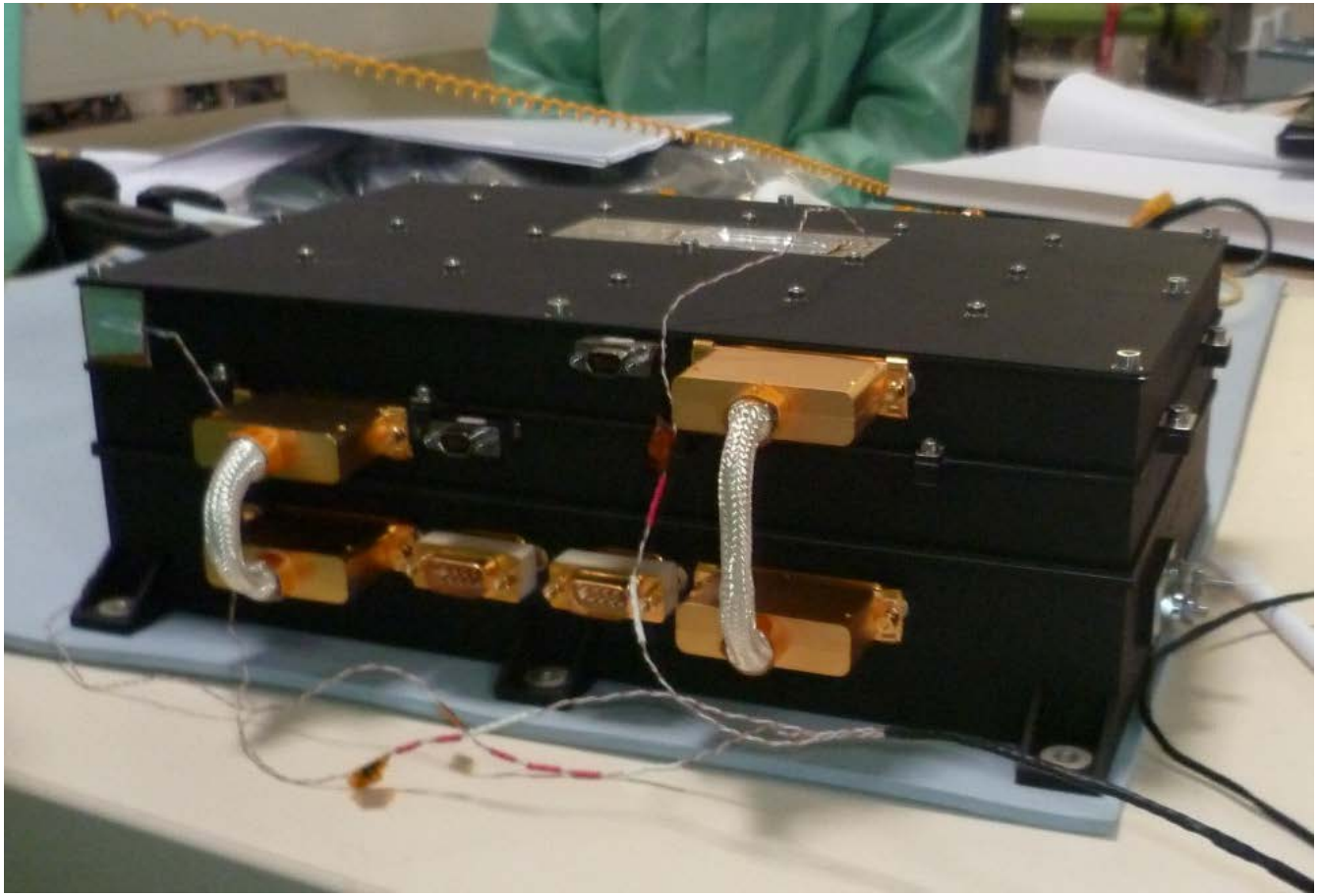
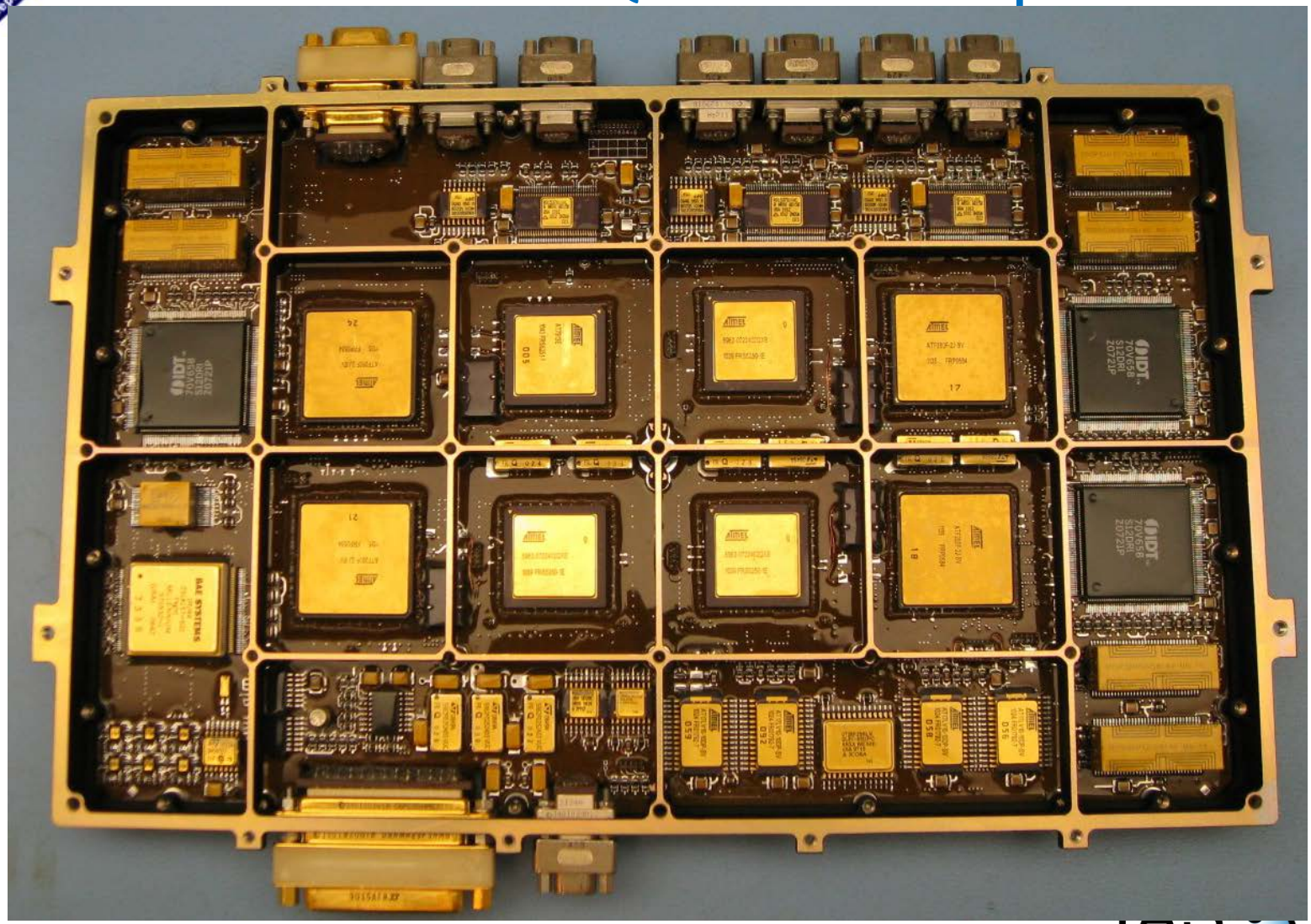


Nominal QM - DPU Top



Nominal QM - DPU Bottom

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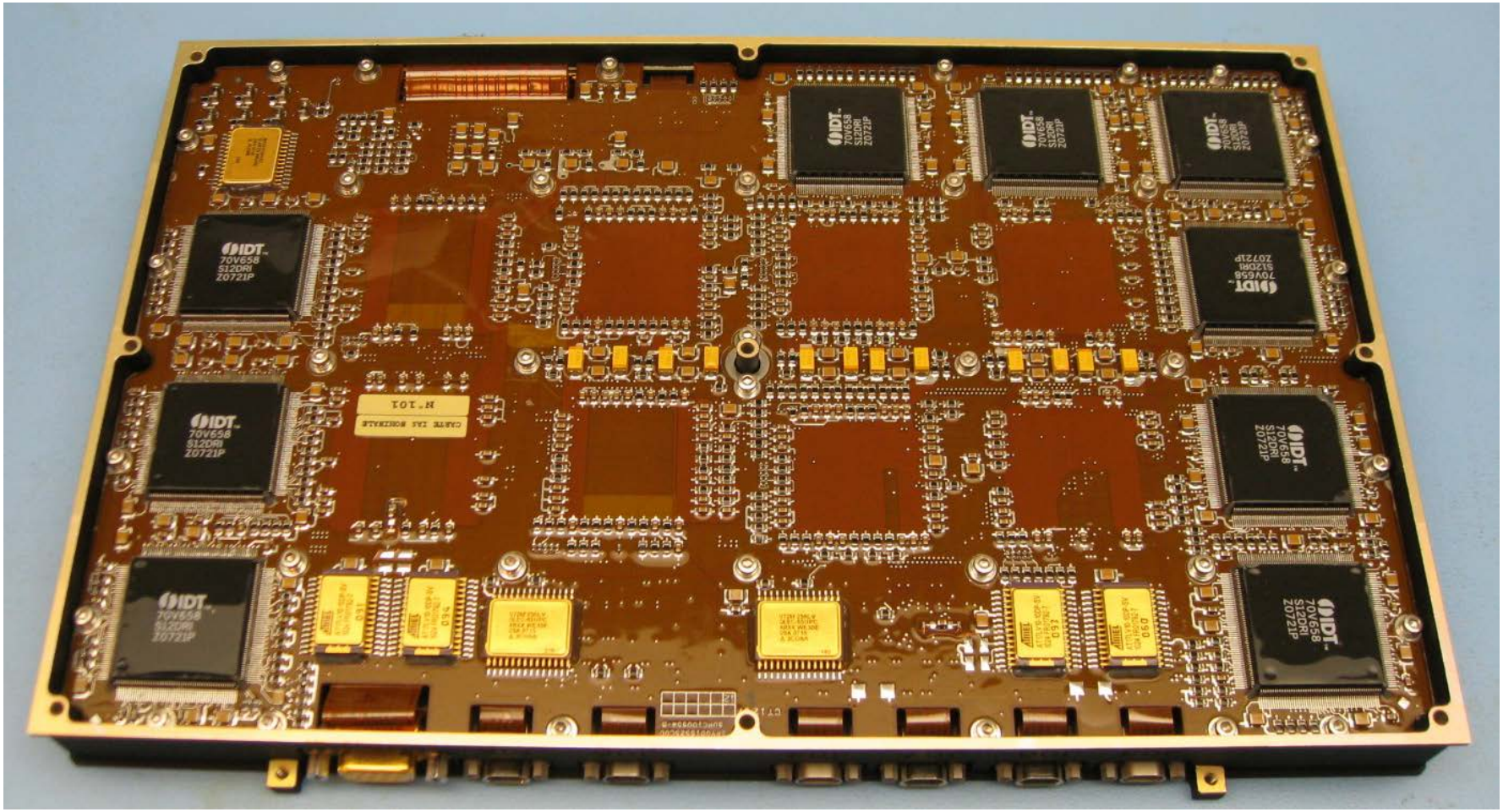

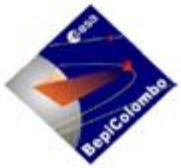

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Thank you for attention

For further questions :

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